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Materials/Processes(1) – Adhesives

A Novel Approach to Incorporate Silica Filler into No-Flow Underfill (*Invited*)
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A Novel Approach to Incorporate Silica Filler into No-Flow Underfill

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Abstract

No-flow underfill technology has been proven to have potential advantages over the conventional underfill technology. However, due to the interference of fillers with solder joint yield, no-flow underfills are mostly unfilled or filled with very low filler loading. The high coefficient of thermal expansion (CTE) of the polymer material has significantly lowered the reliability of flip chip assembly using no-flow underfill, and has limited its application to large chip assemblies. This paper presents a novel approach to incorporate silica filler into no-flow underfill. Two layers of underfills are applied on to the substrate before chip placement. The bottom underfill layer facing the substrate is fluxed and unfilled; the upper layer facing the chip is heavily filled with silica fillers. A design of experiment is implemented to investigate the effect of bottom layer thickness, viscosity and reflow profile on the solder wetting using quartz chip. FB250 daisy-chained test chips are assembled on FR-4 boards using this novel approach. A 100% yield of solder interconnect is achieved with filled no-flow underfill for the first time. Wetting of the eutectic SnPb solder to contact pad on the board is confirmed by Scanning Electronic Microscopy (SEM) and optical microscopic observation. The failure in normal no-flow underfill assembly with silica filler is investigated. The material properites of the bottom layer underfill, upper layer underfill, underfill mixture, and a control sample are characterized. The filled no-flow underfill show a CTE of 40 ppm/°C and a room temperature modulus of 5.2 Gpa. Results indicate that using this novel approach to incorporate silica filler into no-flow underfill, both high yield and high reliability can be achieved. A US provisional patent is filed for this invention.

Introduction

Flip-chip has advantages over other interconnection methods including high I/O counts, better electrical performance, high throughput, and low profile, etc. [1]. It has been practiced in industrial for many years. Recently, the desire for low cost, mass production has resulted in the growing use of organic substrate instead of ceramics. The mismatch in the coefficient of thermal expansion (CTE) between the silicon and the organic substrate causes great thermal stress on the solder joints and shortens their fatigue life. The application of underfill redistributes the thermal stress and enhances the package reliability significantly. [2, 3] However, the current underfilling process encounters various problems. The conventional underfill technology relies on capillary force to draw the liquid underfill into the gap between the chip and the substrate. The capillary flow is usually slow and can be incomplete, resulting in voids. It also produces non-homogeneity in the resin/filler system. The curing of the underfill takes hours in the oven, consuming additional manufacturing time [4]. These problems aggravate further with the increase in chip dimensions and I/O counts, and decrease in gap distances and pitch sizes.

In order to address the problems associated with conventional underfill, several innovative approaches have been developed, or are in development. No-flow underfill technology simplifies the underfill process by eliminating the capillary flow and combining the solder reflow and underfill curing into one step [5]. It has been developed for several years and evaluated in industries. However, due to the interference of silica fillers with solder joint yield [6], no-flow underfills are mostly unfilled or of very low filler loading. The high CTE of the polymeric material limits the package reliability, especially in the case of large dies. Molded underfill is another variation of underfill in development. By adjusting the silica fillers and modifying the process, epoxy molding compound can be molded to fill the gap under the chip [7, 8]. However, the material and process still need to be optimized, and molded underfill is limited to a flip-chip in package. By applying the underfill onto the wafer, wafer level underfill process suggests a convergence of front-end and back-end in package manufacturing and may enable low cost, high reliability flip-chip assembly for high-end applications [9, 10]. The wafer level process presents great challenges to underfill materials. Not only do they have to be compatible with the single flow process similar to no-flow underfill, but also be subjected to wafer level processing such as coating and dicing [11].

For drop-in replacement of conventional underfill process, no-flow underfill technology is a promising solution since it does not require a dramatic change in the semiconductor and surface mount manufacturing. This paper presents a novel approach to incorporate silica filler into the no-flow underfill to reduce the CTE, increase the modulus of the underfill materials and enhance the reliability of flip-chip in large chip applications.

Process Description and Design of Experiment

According to the previous study in the filled no-flow underfill, the cause of the low yield in assembly is mainly the entrapment of silica filler between the solder bumps on the chip and the contact pads on the board, preventing the solders from wetting the pads. It follows naturally that if the fillers can be prevented from entering into the layer between the solder bumps and contact pads, the addition of fillers should not

interfere with the solder joint yield. In this process approach, two layers of underfill are applied. A thin layer of unfilled no-flow underfill with relative higher viscosity is applied onto the board first. Then the liquid no-flow underfill with a high filler loading is dispensed on top of the previous layer. The chip is then placed onto the board and reflowed, during which the solder joints are formed and underfill is cured simultaneously. The process flow is illustrated in Figure 1.

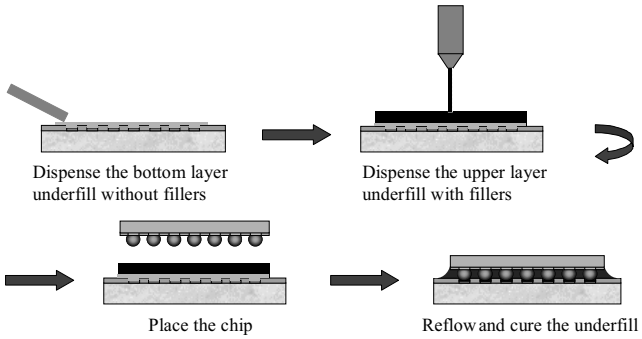

Figure 1. A new no-flow underfill process approach

In order to investigate the effect of process parameters and material properties on the solder wetting, a design of experiment was implemented. The three independent variables were thickness of the bottom layer, viscosity of the bottom layer, and the reflow profile. For each variable, two levels were evaluated. A full factorial experiment was carried out. Each sample conditions are listed in Table 1. The two reflow profiles are shown in Table 2. They were all designed for the seven-zone BTU reflow oven.

Table 1. Details of the experimental design

	Reflow profile	Viscosity	Thickness
#1	Standard	Low	25μm
#2	Standard	Low	50μm
#3	Standard	High	25μm
#4	Standard	High	50μm
#5	Modified	Low	25μm
#6	Modified	Low	50μm
#7	Modified	High	25μm
#8	Modified	High	50μm

Table 2. Temperature settings in the two reflow profiles

Zone	1	2	3	4	5	6	7
Standard	100	150	150	150	180	230	230
Modified	100	150	150	180	230	200	180

The bottom layer underfill (non-filled) was laminated onto Ni/Au coated Cu board first and the thickness was controlled. Then the upper layer underfill (60 wt% filled) was dispensed on top of the bottom layer. The quartz chip bumped with Sn/Pb solder was flipped over and placed on the Cu board. The test vehicle then went through the reflow oven. The bumps were area-array distributed and both the bump height and the bump diameter were 3 mil. After reflow, the wetting of the solder on the Ni/Au coated Cu board was observed under the optical microscope. The pictures are shown in Figure 2.

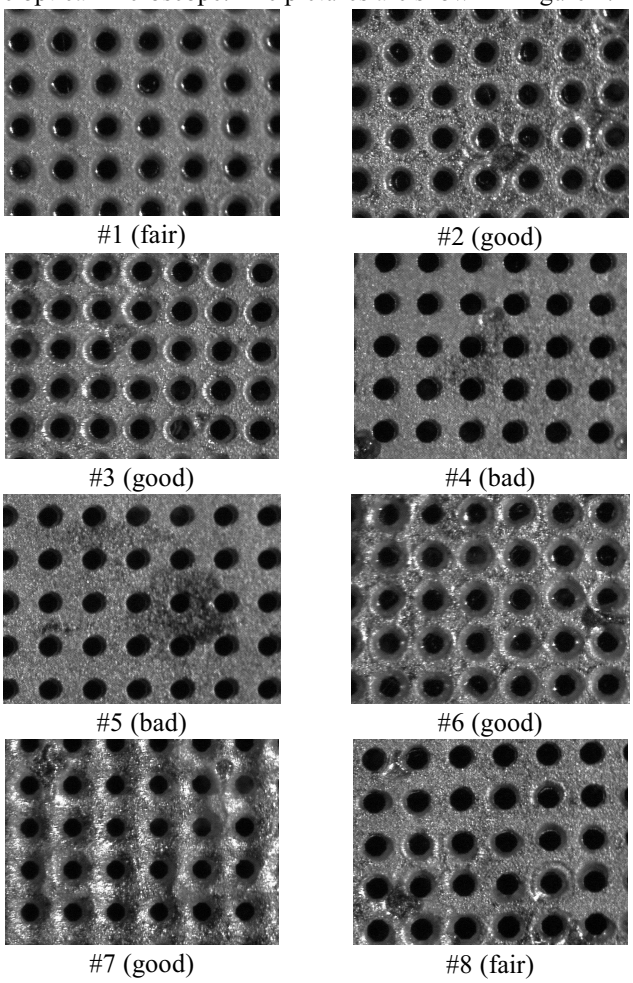

Figure 2. Pictures of quartz chips after reflow

The wetting behavior of the quartz chips can be summarized as the following: When the high viscosity bottom layer underfill was applied, thinner layer showed better wetting; When the low viscosity bottom layer was applied, thick layer showed better wetting; the reflow profile did not have a significant effect on the wetting. The results indicated that the solder wetting process is complicated in this two layer no-flow underfill process. Solder reflow is a dynamic process, and the wetting of solder on the pad will be determined by several simultaneous procedures including the decrease in underfill viscosity, the collapsing of the chip, the settling of the fillers, the curing of underfill, and the solder melting. In the case of low viscosity bottom layer underfill, the low viscosity cannot prevent the fillers from settling down onto the Cu board. So with thinner layer, the filler concentration is higher, which leads to poor solder wetting. In the case of high viscosity bottom layer underfill, if the bottom layer underfill is too thick, it will prevent the chip from collapsing onto the Cu board, causing poor solder wetting.

Assembly

In order to investigate the feasibility of this process, FB250 daisy-chained chips and FR-4 board were used in this study. The chip dimension was 6.3 × 6.3 mm and it had 48

peripheral bumps with pitch size of 18mil. Bump height and diameter was 140 μm and 190 μm, respectively. The solder mask on the FR-4 board was about 40 μm in thickness, and Cu trace about 20 μm. The Cu pads were finished with Ni/Au. They were all designed to be solder-mask-defined in one direction, and pad-defined in the perpendicular direction. The high viscosity bottom layer underfill was printed onto the solder mask opening using solder mask as a natural stencil. Then, a drop of the 65 wt% silica-filled underfill with prescribed quantity was dispensed on the board. The chip was placed on the board and then the whole assembly was reflowed in an Electrovert Omniflo 5 convection reflow Oven. The temperatures in the five zones of the oven were setup as 110°C, 135°C, 200°C, 225°C, and 150 °C, respectively.

Two assemblies were compared in this study. Assembly 1 used the present two layer underfill process, while Assembly 2 used the normal one layer no-flow underfill process. The underfill materials applied in these two assemblies are described in Table 3. In Assembly 1, Underfill BL and UL were applied in sequence according to the previous description. Underfill BL was the bottom layer underfill without silica fillers, and it had the fluxing capability. Underfill UL was the upper layer underfill filled with 65 wt% silica fillers but without fluxing capability. In Assembly 2, a mixture of Underfill BL and UL was applied as a single layer in a normal no-flow underfill process. The reason for the 1:1 volume ratio was that the thickness of the bottom layer was estimated to be 40 – 60 μm according to the measurement from a profilometer, and that the gap distance of the chip to the substrate was around 110 μm according to SEM observation. So Underfill M represented the underfill mixtures that were applied in Assembly 1. Figure 3 shows a picture of assembled chip.

Table 3. Processes and underfills in Assemblies 1 and 2

	Process	Underfill
Assembly 1	Two layer	BL: Bottom layer (unfilled, with flux) UL: Upper layer (65 wt% silica-filled, without flux)
Assembly 2	One layer	M: Mixture (1:1 volume ratio) of Underfill BL and UL

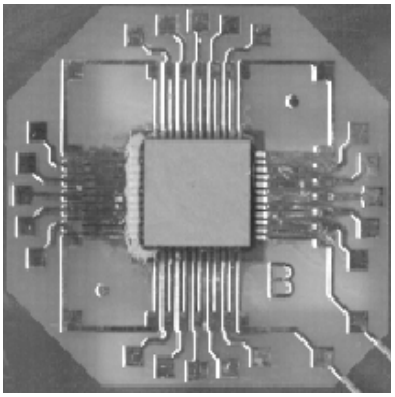

Figure 3. A picture of the assembly

After the reflow, the electrical integrity of the solder joints was tested. Results showed that all the solder joints were interconnected in Assembly 1, while in Assembly 2, none of the solder joints yielded. Although the materials applied as underfill in both assemblies were approximately the same, the new no-flow underfill process had the advantage of high yield. In order to confirm the solder joint integrity in Assembly 1 and to investigate the failure mechanism in Assembly 2, cross-sections of these two assemblies were observed using optical microscope and SEM. Figure 4 shows a SEM picture of a solder joint in Assembly 1. The observation on the silica fillers indicated that although two layers of underfills were applied prior to the solder reflow, there was no discernable separation of these two layers after the reflow. These fillers tended to settle down at high reflow temperature when the viscosity of the underfill decreased. Since the upper layer Underfill UL does not contain fluxing agent, the results showed that the fluxing capability of the bottom layer Underfill BL was sufficient for solder wetting. Figure 5 illustrates an optical microscope observation of a failed solder joint in Assembly 2. The fillers were trapped in between the solder bump and the contact pads, preventing the formation of a solder joint in the reflow process.

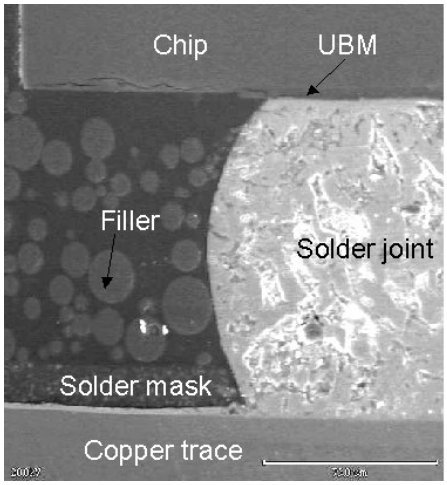

Figure 4. SEM picture of cross-section of Assembly 1

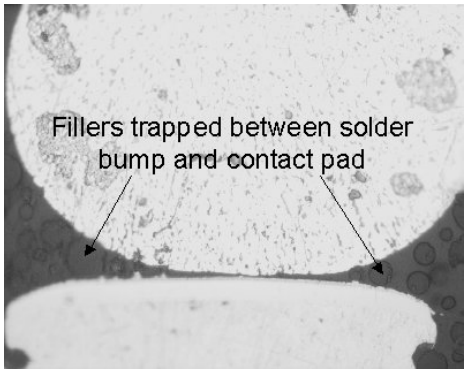

Figure 5. Optical microscope picture of cross-section of Assembly 2

Material Characterizations

The material properties of Underfill BL and UL in Assembly 1, and Underfill M in Assembly 2 were

characterized and compared. A control sample, Underfill C, which was not filled with silica fillers but had fluxing agent incorporated, was also studied. Underfill C represents the normal, unfilled no-flow underfill material.

The filler loading of Underfill M was estimated using Thermo-Gravimetric Analyzer (TGA) by TA Instruments, Model 2050. Figure 6 presents the weight loss of Underfill M during heating in the TGA furnace at a heating rate of at 5 °C/min under N_2 purge. The result suggests that the filler loading in Underfill M was about 55 wt%. Since Underfill M represented the mixture of Underfill BL and UL that were applied in Assembly 1, the actually filler loading of underfill in Assembly 1 was estimated to be around 55 wt%.

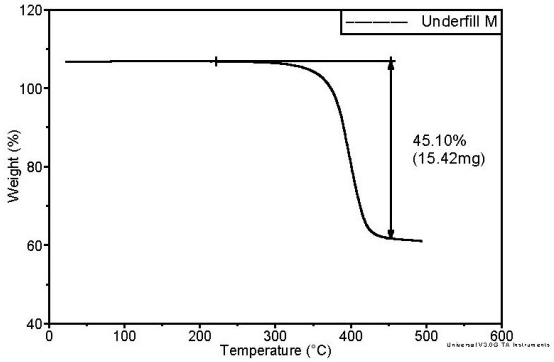

Figure 6. TGA diagram of Underfill M

The curing behavior of the Underfills BL, UL, and M was investigated using a modulated Differential Scanning Calorimeter (DSC) by TA Instruments, Model 2920. A sample of about 10 mg was placed into a hermetic sample pan and heated in the DSC cell at 5 °C/min from room temperature to 300 °C under N_2 purge. The exothermic diagrams of Underfills BL, UL and M are shown in Figure 7. Since two different catalysts were involved in the formulations of Underfills BL and UL, the mixture, Underfill M, displayed a two-step curing behavior.

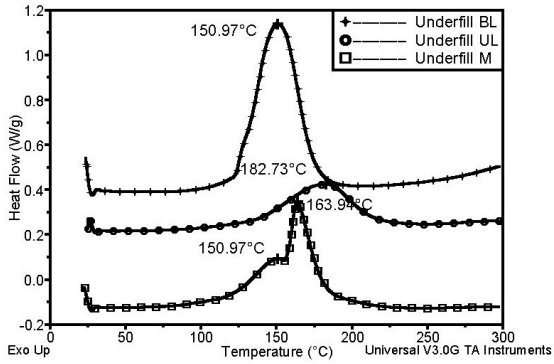

Figure 7. DSC curing profiles Underfill BL, UL, and M

In order to study the material properties of cured underfills, all the samples were cured in a convective oven at 165 °C for an hour. The dynamic moduli of the samples were measured using a Dynamic Mechanical Analyzer (DMA) by TA Instruments, Model 2980. The sample dimension was about 18×6×2 mm. The measurement was performed in a single cantilever mode under 1 Hz sinusoidal strain loading. The samples were heated at 3 °C /min in air to 250 °C. The Coefficient of Thermal Expansion (CTE) of a cured sample was measured using a Themo-Mechanical Analyzer (TMA) by TA Instruments, Model 2940. The dimension of the sample was about 5×5×2 mm. The sample was heated in the TMA furnace to 250 °C at a rate of 5°C/min.

Figure 8 shows the change of storage modulus of Underfills BL, UL, and M with respect to temperature. It can be seen that although Underfill M displayed a two-step curing behavior illustrated by DSC, it only displayed a single Tg transition, indicating that there was no phase separation. Figure 9 compares the storage modulus of Underfill M with that of Underfill C. With fillers incorporated in the resin, Underfill M possessed a high modulus of 5.2 Gpa at room temperature. The thermal expansion behaviors of Underfill M and Underfill C are illustrated in Figure 10. The CTE of Underfill M was around 40 ppm/°C.

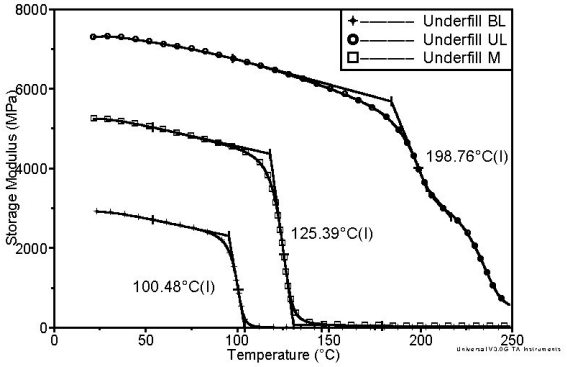

Figure 8. Storage modulus of Underfill BL, UL, and M

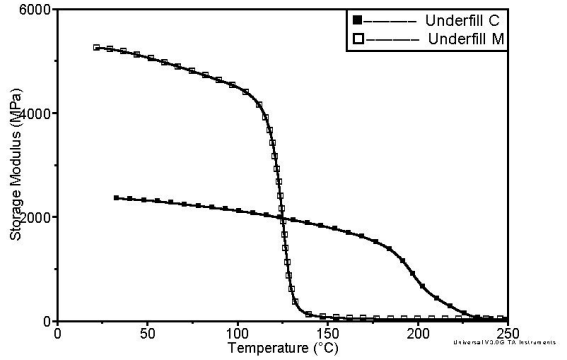

Figure 9. Storage modulus of Underfill C and M

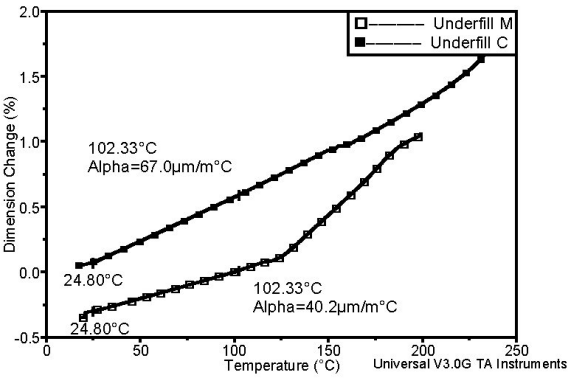

Figure 10. CTE of Underfill M and C

The moisture absorption of cured materials of Underfill M and Underfill C was investigated. The samples were placed into an 85°C/85% RH chamber after they were dried under vacuum at 125 °C over night. The weight changes at different time intervals were recorded and results are shown in Figure 11. Due to the high filler loading in Underfill M, the moisture resistance has been improved significantly.

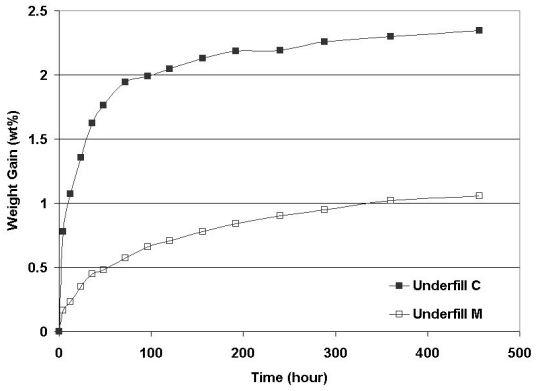

Figure 11. Moisture absorption of Underfill M and C

Conclusions

A novel process has been designed for a high performance filled no-flow underfill for flip-chip applications. In this approach, two layers of underfills were applied onto the printed wiring board before the placement of the chip. The bottom layer was unfilled no-flow underfill and the upper layer was filled with silica fillers. The three-factor experimental design indicated that the thickness and the viscosity of the bottom layer underfill are important parameters affecting the yield of the assembly. Using FB250 bumped chips and FR4 board, high solder joint yield was achieved using the new no-flow underfill process. The normal no-flow underfill process with silica fillers cannot achieve solder joint yield at the same filler loading due to the entrapment of fillers in between the solder bumps and contact pads. The solder joint integrity was examined by SEM and optical microscope observation. The CTE of the filled no-flow underfill was 40 ppm/°C below Tg and the room temperature storage modulus was 5.2 Gpa. This novel process showed a significant potential for a high-yield and high-reliability no-flow underfill process for large-die flip-chip applications. A US provisional patent has been filed for this invention [12].

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A Study of Microwave Curing Process for Underfill used in Flip Chip Packaging. Part 2: 3D FEM Simulation of Microwave Power Distribution inside Variable Frequency Microwave Oven

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Abstract

A three dimensional finite element method was used to simulate the microwave field distribution inside a variable frequency microwave (VFM) oven containing a microwave reflective substrate board. The method was verified first by analyzing two simple cases which have analytical solutions. It was found that the positions of the substrate of flip chip can affect the harmonic frequencies. The power density can be very different at various natural frequencies. It was also found that VFM oven achieve better power distribution. It maybe the first instance to simulate the microwave power distribution for VFM oven.

Introduction

Flip chip packaging, a face down interconnect technique for electronic packaging, can achieve the highest speeds and lowest use of real area of board comparing with other packaging strategies. Flip chips are underfilled by dispensing a liquid along the periphery of the chips. The capillary action then drives it to fill the space. The underfill can reduce relative movement between the silicon chip and the organic substrate caused by CTE mismatch. In general, plastic package materials are thermally cured in hot air. The low conductivity results in low heat transfer rate. Therefore long curing time and low productivity have become the bottleneck in the processing.

Microwave has been used in material processing industry for several decades because of its special energy transfer way. In conventional thermal processing, the energy is transferred into the material through convection, conduction and radiation from the surface. In contrast, microwave energy is delivered directly to materials through molecular interaction with the electromagnetic field. The potential advantages of microwave heating are volumetric and selective heating [1]. The major problems of microwave heating are the spatial non-uniformity of the microwave power, which causes localized hot or cold spots in the applicators. During the material curing process, this non-uniformity of the field intensity can cause burnt or unfully cure of polymers. To overcome or minimize such problems, the field distribution inside microwave oven needs to be investigated. For experimental method, metal components of the sensor can reflect the incident microwave thereafter changes the field distribution, thus the precise measurement of field intensity inside applicators is very difficult. Analytical method can be used to the applicators with regular geometry, but it is not applicable to general applicators, which have both irregular geometry and arbitrary loading.

In the past decade, many researchers used numerical method to simulate the electrical field. FDTD (Finite Difference Time Domain) and FEM (Finite Element Method) were the most useful techniques. The main problems of FDTD are for high Q cavities, the convergence of the FDTD code is rather slow and the solution may take a long time to reach steady state. As a result, the electromagnetic field distribution by FDTD is quite different from the measured one [2]. Because of the obvious advantages with irregular objects, 3D FEM was used to solve the microwave power distribution dissipated in lossy materials in a multimode cavity with fixed frequency. The problem to be solved concerned a rectangular cavity which contained linear, lossy, arbitrarily shaped, isotropic, inhomogeneous materials. The model simulated the curing of composite components well [3, 4].

Comparing with fixed frequency microwave oven, VFM oven has the potential to achieve better power distribution because it sweep the frequency inside a band periodically. Recently, researchers [5,6] have used VFM oven in electronics packaging material processing. However no paper on the simulation of microwave power distribution has been published. For optimizing the curing process, a commercial FEM software, ANSYS5.5 is used in this paper to simulate the microwave field on the surface of a metal-covered substrate in a multi-mode rectangular cavity excited by a source inside a wave-guide. The FEM method and elements are verified by analyzing simple propagation problems which can be solved analytically. To the author's knowledge, this is the first instance to solve the microwave field distribution for curing of polymeric electronic packaging material.

Numerical Model of Microwave Oven

The model used in FEM simulation is given in figure 1. It includes a rectangular cavity (60mm× 70mm×100mm) which contain a reflective substrate at the bottom and a wave-guide (30mm×16mm) at the top. The length of the wave-guide is 40mm. One end of the wave-guide is connected to the cavity and the other end is an open circuit match port. The microwave is generated in a surface which is 10mm far from the match end. The substrate and the oven wall are assumed as perfect conductive surfaces. The dimension of the substrate is 30mm× 20mm×1mm.

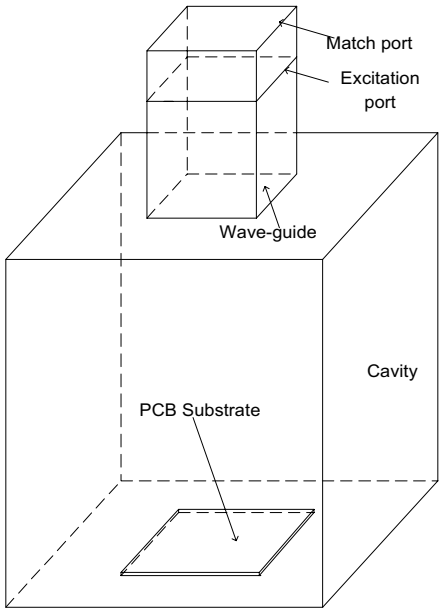

Figure1 Model of microwave oven

Numerical Method

The problem of electromagnetic analysis is actually a problem of solving Maxwell's equations subjected to the given boundary conditions. For general time-varying fields, Maxwell's equations in differential form can be written as:

$$\nabla \times E + \frac{\partial B}{\partial t} = 0$$

$$\nabla \times H - \frac{\partial D}{\partial t} = J$$

$$\nabla \cdot D = \rho$$

$$\nabla \cdot B = 0$$

where E is electric field intensity (volts/meter), D is electric flux density (coulombs/meter^2), H is magnetic field intensity (amperes/meter), B is magnetic flux density (webers/meter^2), J is electric current density (amperes/meter^2) and ρ is electric charge density (coulombs/meter^2).

Another fundamental equation, which is known as the equation of continuity, can be written as

$$\nabla \cdot J = -\frac{\partial \rho}{\partial t}$$

When the field in Maxwell's equations are harmonically oscillating functions with a single frequency, we have a time-harmonic filed. The Maxwell's equations can be written in a simplified form as:

$$\nabla \times E + j\omega B = 0$$

$$\nabla \times H - j\omega D = J$$

$$\nabla \cdot J = -j\omega\rho$$

where ω is angular frequency.

Maxwell's equations become definite when constitutive relations between the field quantities are specified. The constitutive relations describe the macroscopic properties of the medium being considered. For a simple medium

$$D = \varepsilon E$$

$$B = \mu H$$

$$J = \sigma E$$

where the constitutive parameters ε, μ and σ denote, respectively, the permittivity (farads/meter), permeability (henrys/meter), and conductivity (siemens/meter) of the medium. These parameters are tensors for anisotropic media and scalars for isotropic media.

We can obtain the vector wave equation by eliminate H. The governing equation of electromagnetic wave propagation inside oven can be written as:

$$\nabla^2 E - \mu\sigma\frac{\partial E}{\partial t} - \mu\varepsilon\frac{\partial^2 E}{\partial t} = 0$$

The common approach to solve Maxwell equations in a 3D cavtiy with the finite element method has been in the frequency domain via a variational formulation using the functional F [7,4]

$$F(E) = \frac{1}{2}\int_\Omega \left\{\frac{1}{\mu_r}\left|\nabla \times E\right|^2 - k^2\varepsilon_r\left|E\right|^2\right\} d\Omega$$

where $k^2=\mu_0\varepsilon_0\omega^2$, μ_r and ε_r are the relative permeability and permittivity of free space and Ω is the domain being considered. It is assumed here that the fields are sinusoidal function. After discretization, the system can be treated as either an eigenvalue problem to extract the natural frequencies or a boundary value problem to obtain power intensity results for a single excitation frequency.

The boundary condition at a perfectly conducting surface is

$$\hat{\eta} \times E = 0$$

E is the fields exterior to the conductor and $\hat{\eta}$ is the normal direction away from the conductor. A microwave with unit average power and center frequency at 6.425GHz is generated at excitation port. The open circuit match port is a port without reflective wave.

The element used is a ten-node high frequency electromagnetic tetrahedral solid (HF119). There is one DOF associated with each midside geometric node. The element is based on a full-wave formulation of time-harmonic Maxwell's equations in terms of the electric field E (exp(jωt) dependence assumed). The physical meaning of the DOF in this element is a covariant component of E. The element has one DOF on each of its edges and the total number of element DOF is six.

Block lanczos solver can be used to solve the eigenvalue and natural frequency. Based on the harmonic frequencies obtained, Frontal solver can be used to solve the field distribution at resonance.

Results and Discussion

Validation of the Model

To validate the model and FEM method, two simple models that have analytical solutions were tested first. one model was a rectangular cavity (60mm×70mm×100mm) with perfect conductive wall, the central frequency of the sweep source of the microwave oven is 6.425GHz and the bandwidth is 0.2GHz. A FORTRAN program was developed to extract the eigenvalues and natural frequencies based on the famous equation [8]:

$$\left(\frac{l\pi}{a}\right)^2 + \left(\frac{m\pi}{b}\right)^2 + \left(\frac{n\pi}{d}\right)^2 = \left(\frac{\omega_{lmn}}{c}\right)^2$$

where a, b and c are the dimensions of the rectangular oven. l, m and n are integers corresponding to the number of half-wavelengths of quasi-sinusoidal variation of field along the principal coordinate axes, ω_{lmn} is the angular resonant frequency of the l, m and n mode and c is the velocity of light. By this program, the harmonic frequencies, 6.371GHz and 6.500GHz, were obtained. Corresponding modes were 014 and 104 respectively.

Block lanczos solver was used in ANSYS to solve the modes of the rectangular cavity, Table1 gives the harmonic frequencies.

Table 1: Harmonic frequencies by FEM method

Meshing grid	Mode 1 (GHz)	Mode 2 (GHz)
7×7×10	6.380	6.509
8×8×12	6.376	6.504
9×9×15	6.373	6.502

From the results, one can conclude that on one hand, FEM can give very accurate solution, on the other hand, FEM solution converges to the real solutions with smaller elements. When meshing grid was refined to 6.7mm, about 1/7 wavelength, the error of FEM solution is less than 0.15% comparing with the analytical.

The other validation model was a rectangular wave-guide (W×H×L=30mm×16mm×74.35mm). One end of the wave-guide generated the microwave with frequency equaling to 6.425GHz. The other end was a matched port. Since the length of wave-guide equaled to one wave-guide's wavelength, the field intensity at the output end should be equal to the input end. Figure 2 gives the field intensity solution of the wave-guide. Figure 3 gives the comparison of analytical solution, which is a half sinusoid curve, with FEM solutions, horizontal coordinate is the width of the wave-guide. When the element has edge length 3mm (about 1/15 wavelength), the error is less than 5%.

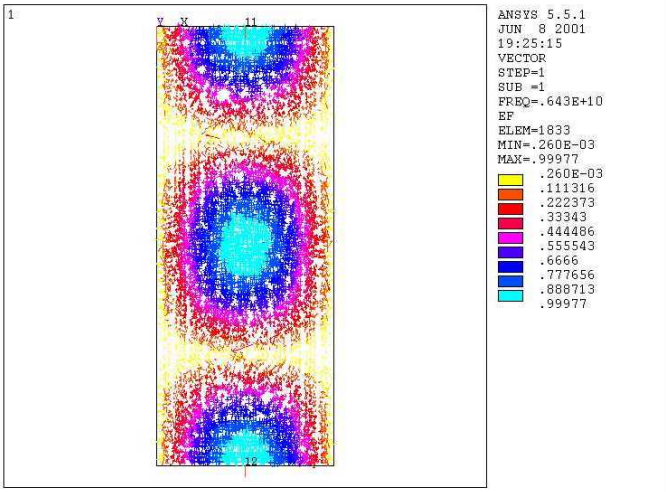

Figure 2 The field intensity solution of wave-guide

Those two elements used in validation model would be used in the analysis of eigenvalue and resonance of microwave oven respectively.

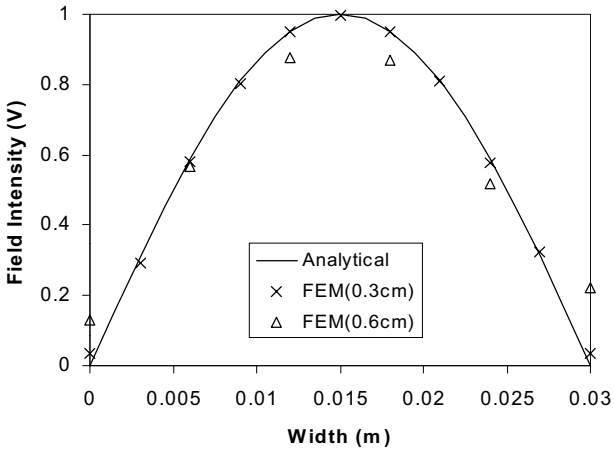

Figure 3: Analytical vs. FEM results

Power Distribution inside VFM Cavity

It is obvious that the position of the substrate can affect the field distribution. The harmonic frequency between 6.325GHz to 6.525GHz was extracted. Table2 gives relationship of the position and harmonic frequency, where D is the distance from substrate to wave-guide port and F is the harmonic frequency. Figure 4 and 5 give the field distribution of the last two cases in Table 2. One can find that the position is very important to the harmonic vibration and field distribution. Sometimes, the substrate can even eliminate the resonance.

Table 2: The effect of substrate's position on F

D(mm)	10	30	40	75	100
F(GHz)	Nil	Nil	6.361	6.243	6.453

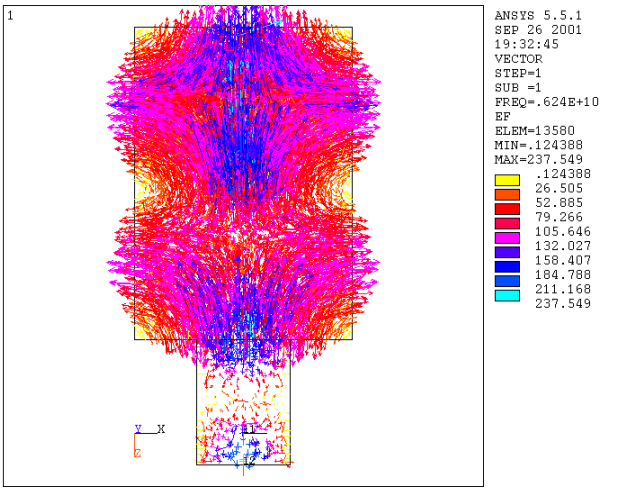

Figure 4 Field distribution at 6.425GHz

Figure 6 and Figure 7 are the power distribution of substrate on the bottom (D=100mm) with two different harmonic frequencies respectively. Table 3 gives the maximum power density nearby 6.4534GHz. When the frequency step is larger than 1 MHz, it is reasonable to use the power distribution at natural frequency to synthesis the power density for the VFM oven, because the peak value of power

intensity is about 100 times larger than the no-harmonic frequencies.

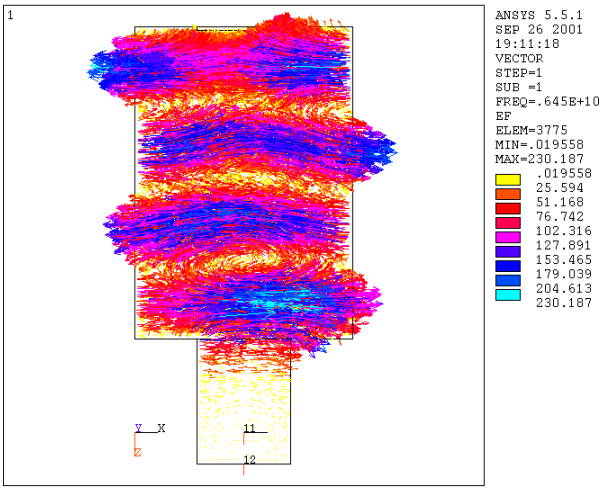

Figure 5: Field distribution at 6.4534GHz

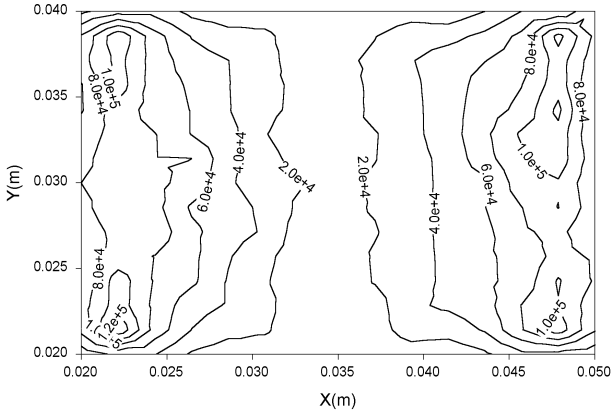

Figure 6: Power intensity (F=6.45GHz)

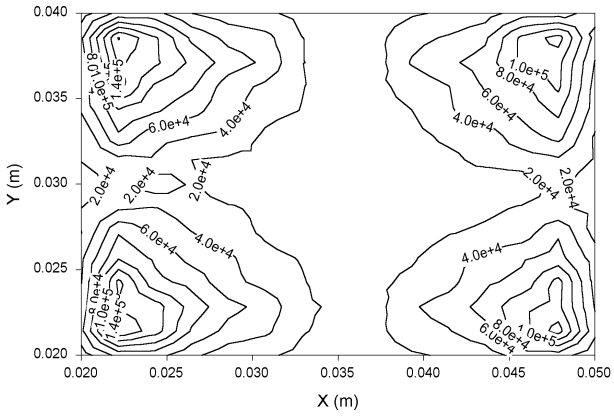

Figure 7: Power intensity (F=6.55GHz)

Table 3: The maximum power density around 6.4535GHz

F(GHz)	6.45	6.4525	6.4534	6.4545	6.457
P(w/m^3)	816	1316	1.39E5	1391	328

There four natural frequencies between 6.4 GHz to 6.6GHz. Those are 6.45GHz, 6.55GHz, 6.57GHz and 6.59GHz respectively. The average power density in this bond is given in figure 5. It proves that more harmonic frequencies can achieve more uniform power distribution. For a VFM oven with dimension 14''×15''×19''(Microcure2100), may have as many as several hundreds natural frequencies, it absolutely can cure the material with more uniform quality than fixed frequency microwave oven.

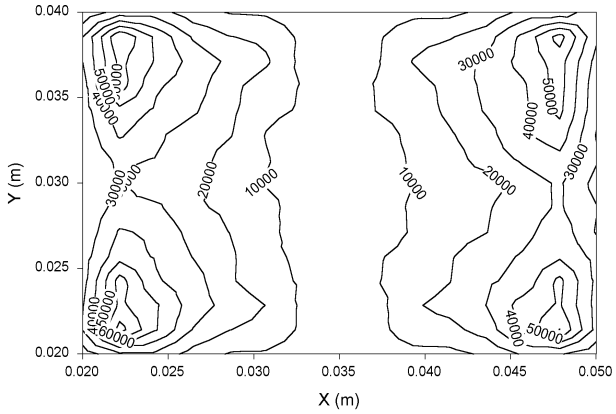

Figure 8: Average power intensity

Conclusion

A commercial 3D finite element method was used to simulate the microwave distribution inside a variable VFM oven.

The method was tested first by analyzing simple problems which have an analytical solution.

It was found that the position of the substrate can affect the harmonic frequency and field distribution.

The power density of VFM oven can be given by the average of the peak powers of the harmonic frequencies. The more the harmonic frequencies in microwave oven, the better field distribution can be achieved. Therefore VFM oven can cure the polymer with better quality than fixed frequency microwave oven.

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High Reliable Non-Conductive Adhesives for Flip Chip Interconnections

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Abstract

Non-conductive adhesives (NCA) are one of the interconnection materials widely used in display packaging and flip chip packaging technology, especially for fine-pitch interconnection. NCA interconnection in flip chip assembly have many advantages such as easier processing, good electrical performance, lower cost, and low temperature processing. In this paper, we have developed new NCA materials, which is film type, for flip chip assembly on organic substrate such as FR-4 printed circuit boards (PCBs). NCAs are generally mixture of epoxy polymer resin without any fillers. As a result, NCAs have higher CTE values than conventional underfill materials used to enhance thermal cycling reliability of solder flip chip assembly on FR-4 boards. In order to reduce thermal and mechanical stress and strain induced by CTE mismatch between a chip and organic substrate, the CTE of NCAs was lowered by filling of non-conductive fillers of diameter below 1 μm. The modified NCA in flip chip interconnection between gold stud bumps of a chip and metal pads of PCB substrates show highly reliable interconnection when exposed to various environmental tests, such as thermal cycling test (-55 ^{o}C/+160 ^{o}C, 1000 cycle), high temperature humidity test (85 ^{o}C/85%RH, 1000 hours) and high temperature storage test(125^{o}C, dry condition).

The effect of fillers on the thermo-mechanical properties of modified NCA materials such as the curing profile, the thermal expansion, the storage modulus, were investigated by using thermal analysis of NCA. In addition, the adhesion of the NCA with different content of filler between gold stud bumped silicon die and FR-4 substrate was measured through die shear test.

The results showed that flip chip assembly using modified NCA materials with low CTEs and high modulus by loading optimized content of non-conductive fillers exhibited good electrical, mechanical and reliability characteristics, that can open wide application of NCA materials for fine pitch flip chip interconnection.

1. Introduction

As the improvement of electronic devices proceeds on, the electronic packaging technology trends move toward lower cost, finer pitch, higher electrical performance, and better reliability. As a result, flip chip technology gains popularity as one of the best chip packaging candidates to meet these trends.

Although flip chip assembly using solder balls is in the main stream of flip chip technology, flip chip assembly using conductive adhesives such as isotropic conductive adhesives (ICAs) and anisotropic conductive adhesives (ACAs) has been under development because of their potential advantages compared with soldered bumps. [1] ~ [3] Some advantages of ACA flip chip assembly are (1) lower processing temperature (epoxy curing less than 150 ^{o}C compared with 240 ^{o}C solder reflowing temperature), (2) finer pitch interconnect (less than 50 μm pitch achieved at chip on glass (COG) technology), (3) lower cost due to less processing steps, and (4) green process (no lead, fluxes, and cleaning solvents).

NCAs, basically materials composed of an adhesive polymer resin and curing agent, have brought much attentions as an alternative for flip-chip-chip on organic boards.

For the full implementation of flip chip using NCAs, it is necessary to provide good reliability data to prove the availability of NCAs flip chip technology. The most commonly observed flip chip failure is occurred during the thermal cycling test, which is due to the thermal expansion mismatch between chips and substrates. Therefore, underfill materials with matched coefficient of thermal expansions (CTEs) between chips and substrates are needed to guarantee better reliability. However, underfill materials cannot be used for NCA flip chips, because chips are directly attached to substrates using NCAs. Therefore, the problem of CTE mismatch between chips and substrates becomes serious with the NCAs flip chip assembly because of high CTE of NCAs materials. For this reason, we have developed the new inorganic filler added NCAs which function not only mechanical interconnection but also the underfill at the same time. Our previous study showed that low CTE adhesive layer with high filler content had lower shear strain induced by CTE mismatch between the chip and the board under temperature cycling. [4]

The purpose of this study is to investigate the effect of added inorganic fillers on NCAs materials characteristics, reliability.

2. Experiments

2.1 NCA Materials

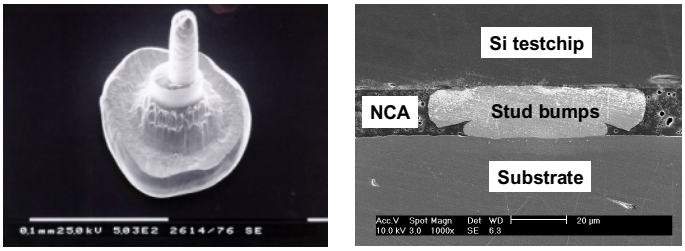
Silica fillers of different content were mixed with liquid epoxy to produce NCAs of 0 wt.% ~ 50 wt.% total filler content. Surface modification of fillers was performed to get uniform dispersion of filler inside epoxy matrix of NCA

composite. NCAs were formulated by mixing fillers, liquid epoxy resin, and a hardener. The mixtures were stirred and degassed under a vacuum for 3 hours to eliminate the air induced during stirring. The cured NCA samples were prepared by placing the adhesive mixture in a convection oven at 150 ^{o}C for 30 min and cutting with 0.6 mm thick dimension for the thermo-mechanical characterization such as thermo-mechanical analysis (TMA), thermo-gravimetric analysis (TGA). And the uncured NCA adhesives were also prepared to interconnect flip chip on organic substrates.

2.2 Bump formation

It is necessary to form bumps on the I/Os of the chip to be interconnected on the substrate using NCA materials.

At first, the gold stud bumps were formed on each I/O pad of test chips using a modified wire bonding machine. The bump has an acute tail, as shown in Fig. 1 (a), to provide good metal to metal contact during thermal compression. It was previously reported that an acute tail bump was more stable than a flat tail bump. [5]



(a) (b)

Figure 1. Scanning electron microscopy of (a) Au stud bumps formed on Al pads of test chip, (b) flip-chip bonded structure

2-3. Flip Chip Assembly using NCA

The modified NCAs in this study consist of an insulating epoxy thermosetting adhesive and non-conductive fillers. Adhesive flip chip bonding was performed using modified NCA for reliability test.

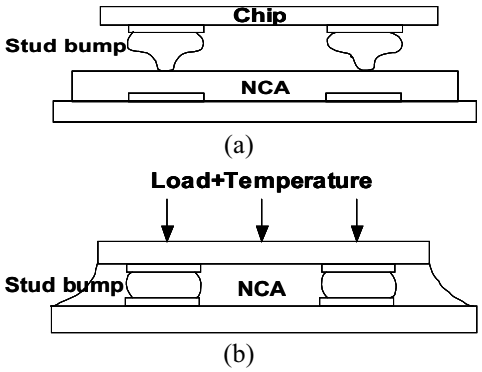


Figure 2. Schematic of flip chip bonding process using NCA (a) NCA application and align, (b) Thermo-compression bonding.

There are three process steps for the NCA flip chip assembly on an organic substrate. First, the gold stud bumps on the chip and the I/O pads on the test substrates were aligned. And then the NCA was dispensed on the substrate to interconnect the chip. Finally, bonding pressure of 2 ~ 3 kgf/cm^2 and temperature of 150^{o}C for 5min was applied to bond the chip on the substrate. Thus the chip is electrically connected to the substrate via conductive stud bumps on test-chip as shown in Fig.1 (b). Non-conductive fillers do not contribute the electrical contacts. Fig. 2 shows schematic of flip chip bonding process using NCA.

2-4. Reliability Test

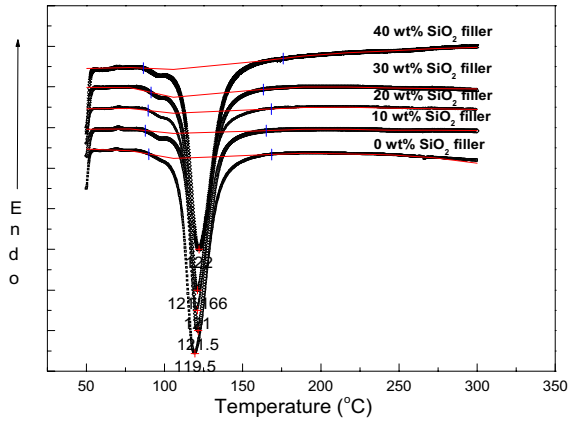
The test chip dimensions 8mm×16mm×0.6mm. It has peripheral-arrayed pads. To investigate the reliability of NCAs flip chip on an organic substrate, contact resistance of a single interconnect is the most important characteristic. The initial contact resistance was measured using a 4-point probe method and after each time interval, in-situ contact resistance were measured during the completion of reliability tests. For the reliability test conditions, 85^{o}C/85%RH high humidity and temperature condition for 1000 hours, 125^{o}C/dry high temperature/dry condition for 1000 hours, and –55^{o}C to 160^{o}C thermal cycling for 1000 cycles condition were adapted.

3. Results and Discussion

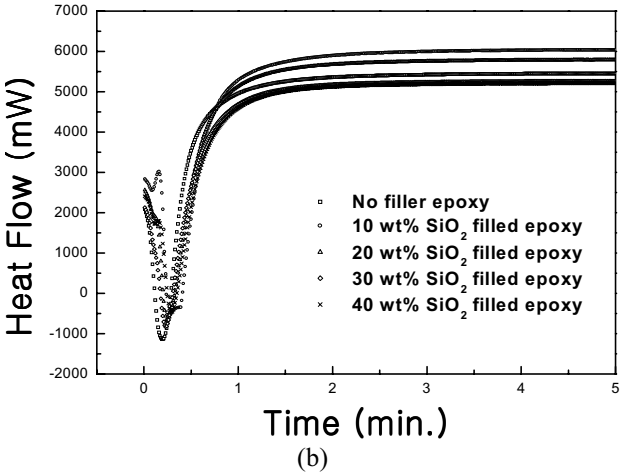
3-1. Material Characterization

3-1-1 DSC results

The DSC curves in Fig. 3 show the effect of filler contents on the curing profiles of NCA composite materials. From the dynamic scan results, similar curing behaviors of different NCA composite materials were observed. However, the increase in the filler content slightly shifted the curing onset temperature and peak temperature to the higher temperature as shown in Fig. 3 (a). For NCA materials with different silica content, isothermal scan was performed. It can be shown that the time to fully cure NCA composite with different silica content was inside 1min.



(a)



(b)

Figure 3. DSC curves of modified NCA samples with different silica contents. (a) Dynamic scan and (b) Isothermal scan of different silica contents NCA composites.

3-1-2. TMA results

CTEs of NCA composite materials with different filler contents were measured using TMA (TA Instrument). The inflection point of thermal expansion curve is defined as TMA Tg (Tg ^{TMA}). This results shows that higher filler content cause the increase in Tg ^{TMA} of the cured samples due to stiffening effect of composite materials with the higher interface area between fillers and epoxy resin as discussed in DMA results. The CTE of the NCA composite below the Tg ^{TMA}, defined as $\alpha 1$, and the CTE above the Tg ^{TMA}, defined as $\alpha 2$, are important parameters in determining the reliability of the NCA flip chip assembly.

Table 1 indicates that the filler content has significant effect on the $\alpha 1$, but no noticeable effect on the $\alpha 2$. From the Tg ^{TMA} and the CTE behaviors, higher content of filler is desirable for the reliability improvement of ACA flip chip assembly.

Table 1. Tg ^{TMA} and CTE of NCA composites below and above Tg ^{TMA}

NCA composite	Tg^{TMA}(°C)	$\alpha 1$ (ppm/°C)	$\alpha 2$ (ppm/°C)
NCA with 0 wt% filler	112.62	69.9	4500
NCA with 10 wt% filler	116.53	61.9	1400
NCA with 30 wt% filler	119.77	41.3	585
NCA with 30 wt% filler	121.91	38.6	263

3-1-3. TGA result

The thermogravitational analysis was performed to evaluate the decomposition temperature of NCA composites with different content of fillers. The decomposition temperatures of three NCA composites were almost that same at 400 °C due to same epoxy resin used. The filler content in NCA composite doesn't influence on the decomposition temperature. Fig. 4 indicates weight loss increases as the filler content decreases.

Furthermore these decomposition temperatures were also similar to those of commercial underfill materials. The decomposition temperature is one of important properties for reworkable underfill used in flip chip package. [6]

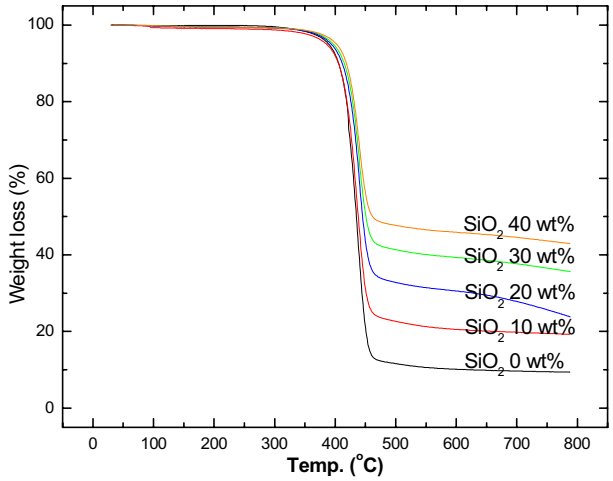


Figure 4. TGA curves of modified NCA samples with different content fillers

3-1-4. Die shear test results

The NCA bonding adhesion between Si/SiO_2 testchip (3mm×3mm) and FR - 4 substrate was measured through die shear test.

A set of typical die shear force – displacement curves of NCA flip chip bonded test-vehicles is shown in Fig. 5 for modified NCA with different silica content. It can be seen that the shear force of test-vehicles using NCA with higher silica content is smaller than that of test-vehicles using NCA with lower silica content. This is because the modulus of NCA with high silica content is larger than that of NCA with low silica content and the relative fracture toughness of NCA with high silica content is smaller than that of NCA with low silica content.

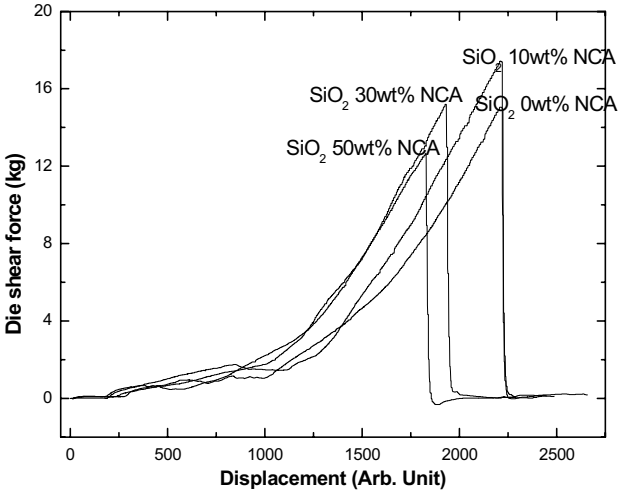


Figure 5. Die shear force – displacement curves of NCA flip chip bonded test-vehicles

Therefore, by considering modulus & toughness, optimal silica content should be determined for better mechanical property of NCA flip chip assembly.

3-2. Reliability Test Results

From thermo-mechanical properties such as curing kinetics, CTE, thermal stability and adhesion, it can be reported optimum silica filler content filled into epoxy matrix is about 30wt%. Modified NCF including silica 30wt% was used and compared with commercial ACFs for reliability test.

Open occurrence rate was defined as the electrical open probability.

The open occurrence rate variations of flip chip assembly using modified NCA composites during 85 °C /85% relative humidity condition for 1000 hrs were shown in the Fig. 6. The open occurrence rate of modified NCA were in acceptable range of around 10% during 85 °C /85% relative humidity condition for 1000hrs when compared with with other commercial ACF for flip chip applications. No catastrophic failure was observed.

And open occurrence rate of NCA flip chip assembly was stable up to 1000hrs during 125°C/dry condition as shown in Fig. 7.

The comparison of reliability results between the 85 °C /85% relative humidity condition and the 125 °C / dry condition reveal that the increase of open occurrence rate of NCA flip chip assembly is mainly due to the moisture attack on the adhesive layer. This effect of moisture attack on open occurrence rate of NCA joint was predominant in case of high moisture absorption rate epoxy resin.

Fig. 8 shows the open occurrence rate of NCA flip chip assembly during –55°C ~ 160°C thermal shock test. The flip chip assembly using commercial ACF-B could not pass 400cycles, and the assembly using modified NCA and commercial ACF-A could pass 700 cycles. These results of thermal shock test indicate that the thermo-mechanical property of NCA composite has noticeable effect on the reliability of NCA flip chip assembly on an organic substrate. Table 2 shows the CTE values characterized by TMA.

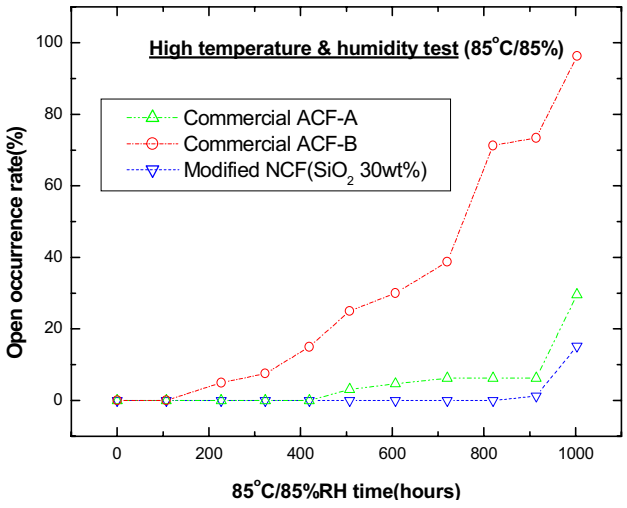


Figure 6. Open occurrence rate of adhesive flip chip interconnects during 85 °C /85%RH test

From thermal shock test result and CTE data, it can be concluded that low CTE (α1, α2) NCA resulted in a better reliability of NCA flip chip assembly on organic substrate during thermal shock test. But, though two adhesive layers have the similar α1 value, adhesive layer with the lower α2 value results in a better thermal shock resistance.

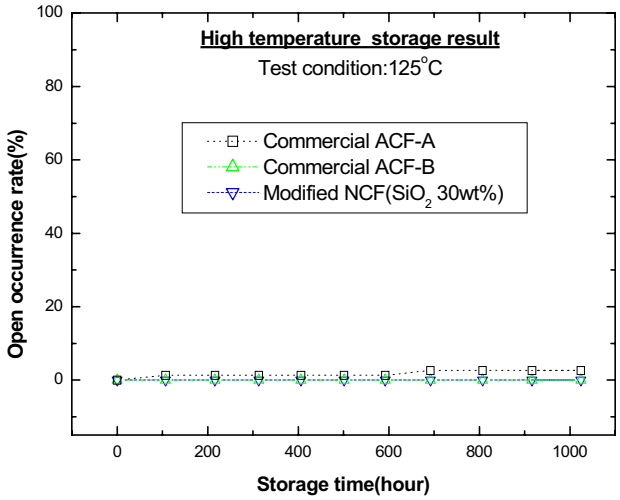


Figure 7. Open occurrence rate of adhesive flip chip interconnects during 125°C high temperature storage test

Table 2. Tg ^{TMA} and CTE of NCA composites below and above Tg ^{TMA}

NCA composite	Tg^{TMA}(°C)	α1 (ppm/°C)	α 2 (ppm/°C)
Modified NCA	119.77	41.3	585
Commercial ACF-A	113.53	38.5	221
Commercial ACF-B	111.77	74.2	1420

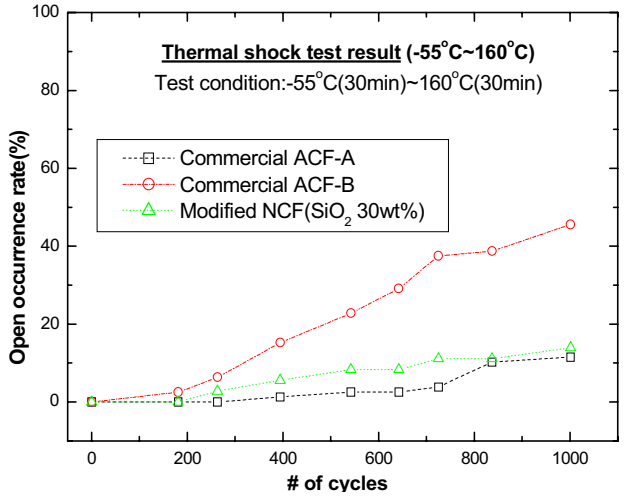


Figure 8. Open occurrence rate of adhesive flip chip interconnects during –55°C ~ 160°C thermal shock test

4. Conclusions

In this paper, the effect of non-conducting silica filler of the NCA composite materials on the curing behavior, thermo-mechanical properties, and reliability for the NCA flip chip assembly on an organic substrate was investigated. The content of non-conducting filler is a key factor which controls the basic properties of NCA composite materials such as curing profile, Tg, CTE, modulus, and adhesion and eventually the reliability of NCA flip chip assembly. The addition of non-conducting filler does not greatly affect the curing kinetics and thermal stability. However, addition of non-conducting filler does noticeably affect CTE, modulus and adhesion.

Therefore, by considering basic material properties, optimum silica content was selected and modified NCA was formulated for reliability test.

These effects of non-conducting filler addition on the NCA material properties were verified by reliability tests. The reliability of NCA flip chip assembly using modified NCA with non-conducting filler is significantly better than that of flip chip assembly using commercial ACF.

Conclusively, the incorporation of non-conductive fillers in the NCA composite material significantly improves the materials property of NCAs resulting in a better reliability of NCA flip chip assembly on an organic substrate.

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